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YAMADA, et al., 10/759,193   500.43408X00 / W1293-01EK
19 January 2007 Amendment   Page 2
Responsive to 19 October 2006 Office Action

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the

application:

Listing of Claims:

1. (Currently Amended) A modular computer system formed by connecting a

processing module having a processor mounted thereon and a plurality of I/O

modules in a stacked form via connectors, where differing ones of the plurality of I/O

modules being differing types of I/O modules from one another, which operate with

mutually differing types of bus-layout configurations, and where at least a portion of

said connectors representing forming a reconfigurable generic bus, wherein

        each I/O module comprises:

        a module exclusive selection part for activating the module responsive

to a module select signal input from a terminal in a predetermined position on a

processing module side connector, the predetermined position being the same for

said I/O modules; and

        an ID output part for outputting identification information of its own I/O

module to at least one predetermined terminal on the connector on the basis of the

module select signal output from said module exclusive selection part;

        wherein said processing module comprises:

                a module select signal output part for outputting the

                module select signal to a connector terminal to which the I/O

                module is connected; and

                an ID input part for taking in the identification information

                output to the at least one predetermined terminal on the

                connector,

where said module select signal output part outputs the

module select signal successively to the I/O modules connected

to the processing module, and

said ID input part recognizes the I/O modules and the

identification information in association ~~in accordance~~ with an

output order of the module select signal; and

wherein in accordance with the association of the I/O modules with the

identification information, <u>for each differing type of I/O module stacked via the</u>

<u>connectors,</u> said processing module selects from differing preset bus-<u>layout</u>

configuration<u>s</u> ~~parameters~~ and device ~~drivers,~~ <u>drivers</u> from a memory, <u>to dynamically</u>

<u>reconfigure the reconfigurable generic bus</u> for accessing the differing <u>type of I/O</u>

<u>module.</u> ~~types of the I/O modules.~~

2. - 4. (Canceled)

5. (Currently Amended) The modular computer system according to claim 21,
wherein

said module exclusive selection part has a plurality of wires connected

to a plurality of connector terminals of the input connector on the processing module

side,

one of the wires is connected to said ID output part, and

one of other wires is connected to a terminal that is included in a

plurality of connector terminals on the ~~ouput~~ <u>output</u> connector, and that is in the

same position as that of the connector terminal supplied with a module select signal

that selects its own module.

6. (Previously Presented) The modular computer system according to claim 21, wherein said module exclusive selection part is formed by connecting a D terminal of a D type flip-flop to one of connector terminals on the input connector, connecting a Q output terminal of said D type flip-flop to said ID output part and to a terminal that is included in the output connector and that is in the same position as that of the connector terminal to which the D terminal is connected, and connecting a clock terminal of said D type flip-flop to a terminal to which connector terminals on the input connector and output connector are connected in common.

7. (Original) The modular computer system according to claim 6, wherein said processing module drives the connector terminal to which the clock terminal is connected, with a clock signal, and drives the connector terminal to which the D terminal is connected, with an enable signal.

8. (Previously Presented) The modular computer system according to claim 21, wherein said ID output part comprises:

an ID generation part for generating identification information of its own module; and

an output enable part for outputting the identification information generated by said ID generation part to a predetermined terminal on the input connector.

9. (Canceled)

10. (Previously Presented) The modular computer system according to claim 21, wherein said ID generation part generates the identification information as a serial signal on the basis of the activate signal and a clock signal.

11. (Previously Presented) The modular computer system according to claim 21,
wherein said ID output part is formed by connecting wires driven by the activate
signal to a plurality of predetermined terminals on the connector via PN-junction
elements according to the identification information.

12. – 20. (Canceled)

21. (Currently Amended) A modular computer system formed by connecting a
processing module having a processor mounted thereon and a plurality of I/O
modules in a stacked form via connectors, where differing ones of the plurality of I/O
modules being differing types of I/O modules from one another, which operate with
mutually differing types of bus-layout configurations, and where at least a portion of
said connectors representing forming a reconfigurable generic bus, wherein
            each I/O module comprises:
            a module exclusive selection part for determining whether a module
select signal input from a processing module side input connector is a signal that
selects its own module, outputting an activate signal when the module select signal
is the signal that selects its own module, and transmitting the module select signal to
a terminal that is included in terminals on an output connector opposite to the
processing module and that is in the same position as that of a terminal on the input
connector supplied with the signal that selects its own module, when the module
select signal input from the input connector is a signal that selects another module;
and
            an ID output part for outputting identification information of the I/O
module to at least one predetermined terminal on the input connector responsive to
the activate signal;

wherein said processing module comprises:

a module select signal output part for outputting the module select signals to the input connector to which a first I/O module is connected;

an ID input part for taking in the identification information output to the <u>at least one</u> predetermined terminal on the input connector,

<u>where</u> said module select signal output part outputs the selecting module select signal successively to the I/O modules coupled to the processing module, and

said ID input part recognizes the I/O modules and the identification information in association ~~in accordance~~ with an output order of the selecting module select signal; and

wherein in accordance with the association of the I/O modules with the identification information, <u>for each differing type of I/O module stacked via the connectors,</u> said processing module selects from differing preset bus-<u>layout</u> configuration<u>s</u> ~~parameters~~ and device ~~drivers,~~ <u>drivers</u> from a memory, <u>to dynamically</u> <u>reconfigure the reconfigurable generic bus</u> for accessing <u>the</u> differing <u>type of the I/O</u> <u>module.</u> ~~types of the I/O modules.~~

22. (New) A modular computer system formed by connecting a processing module having a processor mounted thereon and a plurality of I/O modules in a stacked form via connectors, where differing ones of the plurality of I/O modules being differing types of I/O modules from one another, which operate with mutually differing types of bus-layout configurations, and where at least a portion of said connectors representing a reconfigurable generic bus, wherein

each I/O module comprises:

a module exclusive selection part for activating the module responsive to a module select signal input from a terminal in a predetermined position on a processing module side connector; and

an ID output part for outputting identification information of its own I/O module to at least one predetermined terminal on the connector on the basis of the module select signal output from said module exclusive selection part;

wherein said processing module comprises:

a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected; and

an ID input part for taking in the identification information output to the at least one predetermined terminal on the connector,

where said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing module, and

said ID input part recognizes the I/O modules and the identification information in association with an output order of the module select signal; and

wherein in accordance with the association of the I/O modules with the identification information, for each differing type of I/O module stacked via the connectors, said processing module selects from differing preset bus-layout configurations and device drivers from a memory, to dynamically reconfigure the reconfigurable generic bus for accessing the differing type of I/O module.

23. (New) The modular computer system according to claim 1, wherein said processing module selects from differing preset bus timing sequences from a memory, to dynamically reconfigure a timing sequence operational on the reconfigurable generic bus.

24. (New) The modular computer system according to claim 21, wherein said processing module selects from differing preset bus timing sequences from a memory, to dynamically reconfigure a timing sequence operational on the reconfigurable generic bus.

25. (New) The modular computer system according to claim 22, wherein said processing module selects from differing preset bus timing sequences from a memory, to dynamically reconfigure a timing sequence operational on the reconfigurable generic bus.